Materials for Microelectronics

Advanced materials, microelectronic component configurations and advanced manufacturing methods are required for next generation chips and interconnects to meet the increasing computational demands of AI applications which have changed the paradigm for computational speed and capabilities. This virtual mini-symposium will discuss the challenges and opportunities relative to high-performance computing focusing on materials for microelectronics which are being designed to enable energy efficient and environmentally tolerant computing architectures to meet this rapidly increasing need.

Date/Time: October 16, 2025 11:00 AM - 1:00 PM EST.

Registration:

https://nasem.zoom.us/webinar/register/WN_rMEiTFieRjquEakJu0mchg

Agenda:

a. **11:05-11:30**

Semiconductor Materials Innovations for the AI Era – Vijay Narayanan, IBM Fellow & Senior Manager, Materials Innovation for Logic/Chiplets and Analog AI Compute, IBM T. J Watson Research Center

Artificial intelligence (AI) is now pervasive – augmenting our capabilities and enriching our experiences. However, this explosive growth in model size and the concomitant increase in required compute is unsustainable without significant semiconductor innovations across the hardware stack from materials and devices at the transistor level up through packaging. In this talk, materials advances needed to sustain continued CMOS scaling will be discussed, including: advanced transistor gate stacks and middle of the line interconnect & contact metallurgies novel channel materials driven by emerging device architectures; next-generation photoresists for high-NA photolithography, and thermal considerations due to the advent of backside power technologies for continued scaling. Looking beyond transistor performance, enhanced connectivity and scalability using a chiplet approach will be needed in addition to some of the materials challenges and opportunities for innovation which will be key to the seamless integration of disparate compute components. Indeed, materials innovations will be key to developing and sustaining novel compute and advanced packaging technologies to address key bandwidth challenges needed to power the AI of tomorrow.

b. **11:30-11:55**

Silicon carbide as disrupter and enabler in advanced microelectronics and beyond – Elif Balkas, Chief Technology Officer, Wolfspeed

Silicon carbide (SiC) is rapidly transforming the landscape of microelectronics due to its exceptional material properties, including wide-bandgap, high thermal conductivity, large breakdown electric field, and chemical inertness. These attributes make SiC indispensable for high-performance power and RF electronics operating under extreme thermal, electrical, and environmental conditions. However, as SiC devices push performance boundaries, they simultaneously expose critical limitations in conventional microelectronic packaging. Traditional materials and architectures struggle to meet the thermal, mechanical, and reliability demands imposed by SiC's high operating temperatures and power densities. This gap necessitates a new class of materials engineering, encompassing advanced substrates, high-temperature die-attach solutions, thermally robust interconnects, and encapsulants tailored to fully exploit the benefits of SiC.

Beyond power electronics, SiC is gaining momentum in novel application spaces. Its high thermal conductivity and mechanical strength make it a compelling choice for next-generation heat spreaders and thermal interface materials in aerospace, electric vehicles, and high-performance computing systems. Furthermore, single crystal SiC is being explored for optical windows, photonics, and quantum technologies due to its wide transparency range and excellent radiation hardness.

In all these areas, SiC introduces new challenges in materials integration but also enables transformative solutions by redefining performance and design limits. This presentation highlights SiC's dual role as a disruptor, demanding advanced packaging innovation, and as an enabler across a growing spectrum of high-impact technologies. Overall, this talk aims to inspire and inform attendees about industry's commitment to utilizing SiC materials and devices, also to outline key materials research pathways to fully harness its potential.

c. **11:55 – 12:20**

Advancing AI with Energy-Efficient Architectures: Innovations in Fab Process, Packaging, and System Integration – Mark Fuselier Senior Vice- President of Technology and Product Engineering, Advanced Micro Devices

AI-driven workloads are accelerating compute demand at a pace exceeding 4–5x annually, far outstripping traditional scaling under Moore's Law. This growth has collided with real-world power and thermal constraints. Achieving sustainable performance now depends on system-level efficiency, with materials engineering playing a pivotal role.

This talk will explore how advances in packaging and materials have enabled dramatic gains in energy-efficient compute. Key innovations such as 3D stacking with hybrid bonding, high-bandwidth memory integration, and hierarchical interconnects have delivered significant reductions in energy per operation. These breakthroughs are underpinned by new materials for thermal conductivity, dense interconnects, and advanced power delivery.

Looking forward, continued scaling will demand co-packaged optics, ultra-low voltage transistors, and high-density TSVs—all requiring new materials with improved thermal and electrical properties. To meet the energy demands of the next decade's AI workloads, we

must drive innovation across the full materials stack — from substrate to system. This presentation will outline where the industry must focus to deliver the next era of sustainable, high-performance compute.

d. **12:20 – 12:45**

Materials for On-Chip ULSI Micro- to Nanoscale Interconnects – Dan Edelstein, IBM Fellow and Chief Interconnect Strategist, Semiconductor Technology Research and Development, IBM T.J. Watson Research Center (IBM)

This year marks the 28th anniversary of IBM's introduction of multilevel Cu-based ULSI interconnect technology (termed "BEOL" = back-end of the manufacturing line) into high-volume Si microelectronics production. The transition from Al (0.5%Cu) interconnects to Cu did not change the face of computing; it simply re-opened the door for continued Moore's Law/Dennard's Law scaling of IC chips/FET transistors, passing through the brick wall of Al current density and performance limits. This was not a simple change of one material; it was actually a revolutionary upheaval of the entire BEOL design and fabrication technology, as will be described. In addition to Cu's lower resistivity and higher mechanical and electrical reliabilities, the new Cu BEOL fabrication process enabled broad "hierarchical scaling" of the wiring levels. This scaling has served to mitigate parasitic R dispersion, RC delays, and IR-drops from the longer lines. These combinations and innovations have preserved, in a non-impactful manner, global Cu BEOL manufacturability, which is comprised of yield + performance + reliability. At inception, these benefits were touted as being expected to carry Cu BEOL into the "foreseeable future". Today, we are way past that original vanishing point, and are still continuing into the current foreseeable future, though we may need to "plug in" a novel conductor material at the end of the roadmap (e.g. below the "1 nm node"!). Throughout, there has been a fascinating roadmap of incremental innovations in ancillary materials and engineering "tricks", which I will review in detail. I will also cover the proposed continuation of this roadmap, through novel "post-Cu" conductor materials for potential insertion into the future BEOL manufacturing process.

e. **12:45 – 1:00**

Panel Q&A Session.

The speakers:

Vijay Narayanan

Dr. Narayanan received his B.Tech. in Metallurgical Engineering from the Indian Institute of Technology, Madras (1995), and his M.S. (1996) and Ph.D. (1999) in Materials Science and Engineering from Carnegie Mellon University. After completing post-doctoral research at Arizona State University, Dr. Narayanan joined the IBM T. J. Watson Research Center in 2001 where he pioneered High-κ /Metal Gate Research and Development from the early stages of materials discovery to development and implementation in manufacturing. These High-κ /Metal Gate materials form the basis of all recent IBM systems processors and of most low-power chips for mobile devices. Currently, Dr. Narayanan is an IBM Fellow and Senior Manager at IBM Research where he leads a worldwide IBM team developing Analog Accelerators for AI applications and novel materials innovation elements for advanced CMOS Logic & Chiplets. Dr. Narayanan is an IEEE Senior Member and was elected a Fellow of the American Physical Society in 2011. He was awarded the Distinguished Alumni Award from IIT, Madras for the year 2025. He is an author of over 100 journal and conference papers, holds more than 230 US patents, and has edited one book: "Thin Films On Silicon: Electronic And Photonic Applications"

Elif Balkas

Elif Balkas serves as the Chief Technology Officer at Wolfspeed, responsible for building on the company's strong technology foundation in wide bandgap materials, driving technological improvements to yield products with high quality and reliability as Wolfspeed continues to grow as the only pure play, vertically integrated silicon carbide company. During her 19+ tenure with the company, Elif served in a variety of leadership positions in R&D and operations, dedicating most of her time and focus on developing technologies that are scalable for manufacturing purposes and to enable more efficient and powerful electronic systems. Prior to Wolfspeed, Elif served as a scientist at Intrinsic Semiconductor where she was responsible for GaN and SiC epitaxy product development with a focus on high quality and efficient processes. Elif holds a Ph.D. in Materials Science with a minor in Electrical and Computer Engineering from North Carolina State University, specialized in GaN crystal growth via physical vapor transport. Elif is also a graduate of the Chief Technology Officer Program at Wharton School. In July 2024, Elif was appointed to the US Department of Commerce Industrial Advisory Committee (IAC) for the CHIPS for America program.

Mark Fuselier

Mark Fuselier is senior vice president of Technology and Product Engineering at AMD. He is responsible for silicon and packaging technology development and new product introduction engineering. Fuselier has more than 29 years of semiconductor industry experience and has been involved in the development and production of process technology generations spanning from .35 micron through 2nm across multiple fabs and product families. He played a central role in the development and productization of computing solutions such as 2nm, multi-core CPU and GPU SoC integration, heterogenous APUs, 2.5D and 3D chip-packaging, and chiplet System in Package (SiP) integration. Fuselier holds a Master of Science degree in electrical engineering and Master of Business Administration from the University of Texas at Austin. He is a member of IEEE and the Electron Devices Society.

Dan Edelstein

Dr. Edelstein is an IBM Fellow, and Chief Interconnect Strategist in IBM's Semiconductor Technology Research and Development organization. He has worked for 36 years on nearly all aspects of Cu- and Cu/Low-k ULSI multilevel on-chip interconnect (BEOL) and related technologies, for high-performance microelectronics products. Currently he is leading the team on IBM's BEOL Roadmap through future technology nodes. He holds 312 U.S. patents, and has received various forms of high-level recognition, including 4 IBM Corporate awards, a shared 2004 National Medal of Technology, shared "Inventor of the Year 2006" by NYSIPLA, appointed IBM Fellow in 2006, elected to the U.S. NAE in 2011, and shared the 2019 IEEE Cledo Brunetti Award.

Moderators:

Anil Sachdev, retired, General Motors

Daniel Edelstein, IBM